



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2827
Examiner: Luan C. THAI

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Supplementary
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7-2-02

Re PATENT APPLICATION Of:

Applicant(s): Makoto TERUI, et al.

Serial No.: 09/827,246

Filed: April 6, 2001

For: SEMICONDUCTOR APPARATUS
WITH DECOUPLING CAPACITOR

Docket No.: IIZ 122

PRELIMINARY
AMENDMENT

June 26, 2002

Assistant Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir:

Preliminary to examination, please amend the application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 21, please replace paragraph [0080] with the following replacement
paragraph:

--Referring to Fig. 2, a motherboard 9 is manufactured considering organic material, such as glass epoxy, as a base. The motherboard 9 is provided at the inner layer and outer layer with copper wiring patterns. The motherboard 9 is also provided at both upper and lower surfaces with terminals on which semiconductor devices and chips are mounted. A semiconductor device 8 and chips, such as resistances and capacitors, are mounted on the motherboard 9 using solder paste.--

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Page 22, please replace paragraph [0084] with the following replacement paragraph:

A2 --The semiconductor chip 103 is mounted on the die pad 101 using conductive paste 102. In the drawings, "P" represents a power supply terminal and "G" represents a ground terminal. The inner leads 105, connected to the power supply terminals P and ground terminals G, are extended inwardly toward the semiconductor chip 103. A chip capacitor mounting pad 111 is formed at the inner ends of the adjacent two extended inner leads 105. A chip capacitor 110 is mounted on each of the chip capacitor mounting pads 111 using conductive adhesives 112, such as silver-epoxy system adhesives or solder paste. All of the semiconductor chip 103, chip capacitors 110 and inner leads 105 are molded with the mold resin 106 entirely.--

Page 64, please replace paragraph [0202] with the following replacement paragraph:

A3 --According to this embodiment, a copper layer is formed on a surface of an organic material substrate 1821, and the copper layer is etched to form a conductive pattern (wiring pattern) 1822. The wiring pattern 1822 (1822p, 1822g) is connected via through holes 1823 to ball mounting pads 1824, formed on the opposite surface of the organic material substrate 1821. A solder resist 1826 is selectively formed on the both surface of the organic material substrate 1821.--

Page 68, please replace paragraph [0211] with the following replacement paragraph:

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A4 --According to this embodiment, a copper layer is formed on a surface of an organic material substrate 1921, and the copper layer is etched to form a conductive pattern (wiring pattern) 1922. The wiring pattern 1922 (1922p, 1922g) is connected via through holes 1923 to ball mounting pads 1924, formed on the opposite surface of the organic material substrate 1921. A solder resist 1926 is selectively formed on the both surface of the organic material substrate 1921.--

IN THE CLAIMS:

Please cancel claims 1-45 without prejudice or disclaimer to the subject matter recited therein.

Please amend the claims as follows:

A5 46. (Amended) A semiconductor apparatus₁ comprising:
a substrate;
a die pad which comprises a power supply bonding area which is formed by extending outwardly all the sides of the die pad;
ground terminals which are to be grounded;
power supply terminals which are supplied with electrical power;
first conductive patterns which are formed on the substrate and are connected to the ground terminals;
second conductive patterns which are formed on the substrate and are connected to the power supply terminals and the power supply bonding area;
a high dielectric constant layer formed on the die pad; and

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cont

a metal layer formed on the high dielectric constant layer and having a chip mounting area on which a semiconductor chip is mountable and a ground bonding area surrounding the chip mounting area, the ground bonding area being connected to the first conductive patterns.

47. (Amended) A semiconductor apparatus according to claim 46, wherein the metal layer is provided with a ridge surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

48. (Amended) A semiconductor apparatus according to claim 46, wherein the high dielectric constant layer is composed of ceramics.

Please add the following claims:

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--49. A semiconductor apparatus according to claim 46, wherein the high dielectric constant layer is alumina (aluminum oxide) and titan oxide.

50. A semiconductor apparatus according to claim 46, wherein the metal layer is provided with a ridge surrounding the chip mounting area so as to separate the chip mounting area from the ground bonding area.

51. A semiconductor apparatus according to claim 46, wherein the metal layer has a shape that is smaller than a shape of the die pad.

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52. A semiconductor apparatus according to claim 51, wherein the metal layer partially covers the die pad, and wherein the power supply bonding area is a part of the die pad that is not covered by the metal layer.

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53. A ball grid array semiconductor package, comprising:

an substrate;

a die pad which is formed on an upper surface of the substrate, and which comprises a power supply bonding area which is formed by extending outwardly all the sides of the die pad;

ground terminals which are to be grounded;

power supply terminals which are supplied with electrical power;

first conductive patterns which are formed on the upper surface of the substrate and are connected to the ground terminals;

second conductive patterns which are formed on the upper surface of the substrate and are connected to the power supply terminals and the power supply bonding area;

a high dielectric constant layer formed on the die pad;

a metal layer formed on the high dielectric constant layer and having a chip mounting area on which a semiconductor chip is mountable and a ground bonding area surrounding the chip mounting area, the ground bonding area being connected to the first conductive patterns;

ball mounting pads disposed on a lower surface of the substrate;

interconnecting patterns which electrically couple the first and second conductive patterns to respective ones of the ball mounting pads; and

solder balls mounted on the ball mounting pads.

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54. A ball grid array semiconductor package according to claim 58, wherein the metal layer is provided with a ridge surrounding the chip mounting area so as to define the chip mounting area and ground bonding area.

55. A ball grid array semiconductor package according to claim 58, wherein the high dielectric constant layer is composed of ceramics.

56. A ball grid array semiconductor package according to claim 58, wherein the high dielectric constant material is alumina (aluminum oxide) and titan oxide.

57. A ball grid array semiconductor package according to claim 58, wherein the metal layer is provided with a ridge surrounding the chip mounting area so as to separate the chip mounting area from the ground bonding area.

58. A ball grid array semiconductor package according to claim 58, wherein the metal layer has a shape that is smaller than a shape of the die pad.

59. A ball grid array semiconductor package according to claim 63, wherein the metal layer partially covers the die pad, and wherein the power supply bonding area is a part of the die pad that is not covered by the metal layer.--

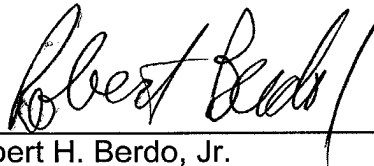
60. A semiconductor apparatus according to claim 46, wherein the substrate includes an organic material.

61. A ball grid array semiconductor package according to claim 53, wherein the substrate includes an organic material.

REMARKS

Claims 1-45 are canceled. Claims 46-48 are amended. Claims 49-61 have been added. Examination of the amended application is respectfully requested.

Respectfully submitted,



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